REMARKS/ARGUMENTS

Claims 6-25 are pending. No claim has been amended, canceled, or added.

Claims 6-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsu in view of Gill and Stewart. Applicants respectfully traverse the rejection.

Claim 6 is directed to a flash memory and relates to a source side programming. Conventional single gate/transistor flash memory devices perform programming operations by charging the floating gate with injection of hot channel electrons from the drain side. The present inventors discovered that source side programming provides improved performance over the conventional drain side programming. As explained on page 6 of the specification, the programming rate distributions for the source side programming are within 10 programming time pulses while that for the drain side programming are as long as 30 pulses (lines 15-20). One benefit of having a shorter and better controlled program distribution for source side programming is that the post-programming threshold voltage distribution for cells in the array is tighter.

Claim 1 recites, "a plurality of floating gate transistors, each transistor having a control gate a floating gate, a drain and a source, said plurality arranged in an N-row by M-column array, where N and M are integers greater than or equal to one; N word lines, each word line connecting together the control gates of transistors in a common and corresponding row; and M bit lines, each bit line connecting together the drains of transistors in a common and corresponding column, wherein a specific floating gate transistor of the plurality is selected and programmed by applying a first voltage to the control gates of the transistors in the row in which the specific transistor is disposed, applying a second voltage to the source of the specific transistor and grounding the drain of the specific transistor."

Hsu is directed to a self-aligned buried channel stacked gate flash memory cell, where the effective channel length dimension is independent of the critical dimensions of the stacked gate structure. Hsu discloses a single-transistor-cell device, where no more than one transistor is required to program a cell. Hsu states that a relatively high voltage (about 12 volts) is applied to the control gate and a moderately high voltage (about 9 volts) is applied to the drain

for a conventional programming operation (col. 1, lines 51-56). It does not provides any motivation or suggestion for modifying this programming operation. That is, it does not suggest performing source side programming, in the manner recited in claim 1.

Gill is directed to a memory cell array for a non-volatile memory device having single-transistor cells that are arranged in a matrix of rows and columns. To perform a programming operation, first programming voltage and second programming voltage are applied to a control gate and drain of a cell, respectively (col. 3, lines 44-49). As with Hsu, Gill does not appear to provide any motivation or suggestion for modifying the programming operation, wherein the source region is biased rather than the drain region.

Stewart is directed to a non-volatile memory having multiple transistors for a single cell (see Fig. 4). To program a bit, at least two transistors Pw and Ps are used. The programming operation involves applying first turning on the transistor Pw that has its source region coupled to the source region of the transistor Ps (col. 4, lines 28-35). After turning on the transistor Pw, a voltage (50 volts) is applied to the control gate of the transistor Ps to program it (col. 4, lines 41-43).

Accordingly, Stewart discloses a non-volatile memory having a very different configuration than that of Hsu and Gill. Unlike Stewart, both Hsu and Gill disclose non-volatile devices of a single-transistor cell type, where no more than one transistor is used to program a cell. Stewart cannot be combined with Hsu and Gill without changing the fundamental configuration of the devices disclosed in Hsu and Gill. For example, it would be difficult to arrange Stewart in a matrix of word lines and bit lines, as disclosed in Gill (see Fig. 1B). In addition, the device of Stewart and those of Hsu and Gill operate in different voltage regimes, 15 volts vs. 50 volts, as a result of the widely different device configuration. Applicant respectively submit there is no motivation to combine Stewart to Hsu or Gill. Claim 6 is allowable.

Claim 14 is directed to a non-volatile device. The claim recites, "a substrate; a floating gate overlying the substrate; a control gate overlying the floating gate and being electrically coupled to a word line extending in a first direction; a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending into the substrate and having a first depth, the drain region having a first graded profile and being

electrically coupled to a bit line extending in a second direction that is substantially perpendicular to the first direction; and a source region provided in the substrate and proximate a second end of the floating gate, the source region and drain region defining a channel therebetween, the source region extending into the substrate and having a second depth that is greater than the first depth, the source region having a second graded profile that is more sloped than the first graded profile, wherein the control gate is applied with a first voltage and the source region is applied with a second voltage to program the non-volatile device." These features are not disclosed or suggested by the cited references. Claim 14 is allowable.

Claim 19 is directed to a non-volatile semiconductor device. The claim recites, "a semiconductor substrate; and a transistor formed on the substrate, the transistor including: a floating gate overlying a surface of the substrate, a control gate overlying the floating gate and being electrically coupled to a first conductive line extending in a first direction, a first conductive region provided in the substrate and proximate a first end of the floating gate, the first conductive region extending a first distance into the substrate and having a first graded profile relative to the surface of the substrate, the first conductive region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and a second conductive region provided in the substrate and proximate a second end of the floating gate, the second conductive region being a double-diffused region that extends a second distance into the substrate and having a second graded profile relative to the surface of the substrate, the second distance being greater than the first distance, the second graded profile having a greater slope relative to the surface of the substrate than the first graded profile, wherein the control gate is applied with a first voltage and the second conductive region is applied with a second voltage to program the non-volatile device, the second voltage being a positive voltage." These features are not disclosed or suggested by the cited references. Claim 19 is allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Steve Y. Cho
Reg. No. 44,612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300

Attachments
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